CMOS image sensor for the analysis of fast moving luminous objects

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ABSTRACT

We present an image sensor dedicated to the analysis of fast moving luminous objects. The circuit is fabricated in standard 0.6\textmu m CMOS technology with an image sensing array of 64 \times 64 pixels. Its working principle is as follows: An electronic unit integrated at the pixel level measures the elapsed time since the beginning of the acquisition till the passage of the luminous object in front of the pixel under consideration. This value that corresponds to a number of clock cycles is stored in a 4-bit memory at the pixel level and translated into a grey level, the brighter ones corresponding to the shortest time. The result is a 16-gray level image that represents the trajectory and direction of motion of the object. Knowing the frequency of the clock, the distance between the pixels and the difference in grey levels of the pixels, the speed of the moving object can be determined. Alternatively, the 16-gray level image can be considered as a superposition of 16 one grey level images that represent the 16 positions of the moving object at 16 different time instances in the course of its displacement. The frequency of the clock can be as high as 20MHz for the analysis of very high speed phenomena. The working principle and the architecture of the image sensor will be described in details in this paper. Moreover, the results of the tests carried out on the circuit, namely the analysis of the movement of the spot on an oscilloscope screen, will also be reported and the potential applications of the image sensor discussed.

Keywords: Image sensor, CMOS, high speed phenomenon

1. INTRODUCTION

Most of the CMOS image sensor developments have been, up to now, directed towards relatively slow speed image capture. But today, there is an increasing interest in the use of such sensors for high speed, high resolution applications that were until recently the exclusive domains of CCD imagers. Besides, contrary to older CMOS sensor architectures such as the passive pixel sensor (PPS) and the active pixel sensor (APS)\textsuperscript{1} which have analog readouts, the more recently developed digital pixel sensor (DPS)\textsuperscript{2} employs a per-pixel analog-to-digital converter (ADC) in order to produce digital data at the output of the image sensor array. In this paper, we describe a 64 \times 64 DPS structure based image sensor with a per-pixel electronic decision unit and digital memory. Our circuit is dedicated to the observation and analysis of fast varying luminous phenomena with time constant smaller than 1\mu s. The innovation in our image sensor resides in the fact that only one image of the moving object needs to be taken and analyzed in order to determine its speed. Moreover, there is a direct relationship between the grey levels of the image and the speed of the moving object. Image acquisition using our sensor is achieved by simultaneously exposing all the pixels under the control of an external clock whose frequency determines the exposure time. The image data are first stored in the memory devices integrated at the pixel level and then readout on the 4 digital outputs yielding a 16-grey level image on which processing is done in order to determine the speed of the observed moving object. The rest of the paper is organized as follows. Section 2 introduces the working principle of the image sensor. Section 3 presents our DPS based sensor architecture and gives its main characteristics. A detailed description of the pixel design is given in section 4 followed by an explanation of the operation of the sensor in section 5. Finally, the experimental tests carried out on the sensor and the results obtained are presented and discussed in section 6.

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2. WORKING PRINCIPLE

The working principle is based on an original DPS pixel architecture (fig.1(a)) that can perform temporal coding. A comparator directly connected to the output of the photo-detector is used to detect the moment the latter falls below a threshold value. When this occurs, the output of the comparator switches from a low logic value to a high logic value. The time delay between the start of acquisition and the moment the output of the comparator changes state depends on the intensity of the luminous flux. However, if the scene under observation is a highly luminous moving object, then, this time delay is negligible and the state change is almost instantaneous as the luminous object passes in front of the pixel. If we are able to measure the elapsed time since the start of acquisition till the moment the comparator output changes state then we know the time that the luminous object took to travel from its initial position at the start of acquisition to that of the current pixel. This is achieved using a common 4-bit counter which is initialized and started counting at the beginning of the acquisition and whose value, at the moment the comparator changes state, is stored in the 4-bit SRAM memory. The memory write signal is a short pulse generated by the pulse generator when a transition is detected at the output of the comparator. The common 4-bit counter is operated by an external clock whose frequency determines the exposure time; the higher the frequency the shorter is the exposure time. So, the frequency is chosen according to how fast is the phenomenon under observation. After 16 clock cycles, that correspond to one turn of the common counter, the latter is locked and the values stored in the memories are readout, transformed into grey levels and displayed as a 16-grey level image. The grey level represents thus the time that has elapsed since the beginning of the acquisition, in terms of clock cycles, before the object passes in front of the pixel. The brighter is the pixel the shorter is the time. Thus, the variations of the grey levels of the pixels allows us to determine the trajectory and direction of motion, and to compute the speed of the moving object.

3. CIRCUIT DESIGN

A photomicrograph of the DPS chip is shown in fig 2(a). The chip contains about 400 thousand transistors integrated on a $3.7 \times 4.3 \mu m$ die. The sensor array is $64 \times 64$ pixels. Each pixel is composed of a photodiode, a comparator, a pulse generator and a 4-bit SRAM as shown in fig 1(a). Its size is $49.2 \mu m \times 49.2 \mu m$ and it contains 55 transistors.

The main functional blocks of the sensor are illustrated in fig 2(b). The core of the sensor is the array of $64 \times 64$ pixels. On the periphery of the array are the 4-bit common counter (a Gray code counter), a control sequencing block, a row decoder, a demultiplexer, a column amplifiers and tristate inverters that control the memory access. A row decoder and demultiplexer are used to transfer signals from pixel's memory to four digital outputs, through column amplifiers.

The sensor has three modes of operation that will be depicted in section 5. These modes are the acquisition mode, the read mode and the write mode. The choice of the mode of operation is done by applying the appropriate
3-bit code to the Cde input bus represented in fig.2(b). Depending on the value of the mode selection code, the Gray code counter and the control sequencing block, working like a synchronous Finite State Machine (FSM), generate in a synchronous way all the control signals required by the DPS circuit to operate in the chosen mode.

4. PIXEL DESIGN

Fig.3(b) represents the schematic diagram of the pixel. The photo-detector circuit is implemented as a diffusion-N well photodiode with a reset, an anti-blooming and a (Read/Write Enable) transistor. The photo-detector architecture is based on charge integration for transducing the photocurrent into a voltage. We have chosen this function mode because it achieves better gain conversion than other modes. The layout of the pixel is represented in fig.1(b). Its fill factor is about 18% for a pixel area of 49.2 µm².

Prior to the acquisition of an image, the photo-diode or its equivalent capacitor must be charged. This is achieved by turning ON the transistor M1 so that the voltage at node Vd is set to the value Vdd resulting in the capacitor being charged up to its maximum analog value, see fig.3(a). The equivalent capacitor is in fact the parasitic capacitor of the photodiode and its capacitance is essentially due to the photodiode size (area and perimeter).

\[ C = K_p \cdot 4a + K_s \cdot a^2 \] with \( a = \text{perimeter}, a^2 = \text{area} \)

and

\[ K_p = 430 \cdot 10^{-12} F/m, \ K_s = 380 \cdot 10^{-6} F/m^2 \] for AMS 0.6 µm technology.

For our photodiode \( a = 529 \mu m \) and the estimated capacitance is \( C = 0.24pF \).

The transistor M1 is next turned OFF in order to start an image acquisition. In this case the parasitic capacitor is discharged and the voltage at node Vd decreases linearly or at constant rate that is a function of the magnitude of the incident luminous flux. When this voltage reaches the threshold value, the output of the comparator switches from a low logic value to a high logic value and a short memory write pulse is generated by the pulse generator (See Vc, Vd and Vp voltage fig.3(a)).

The analog bias voltage Vref is used to limit the blooming phenomenon. This phenomenon occurs when the intensity of the luminous flux is too high resulting in a too rapid decrease of the voltage at the node Vd which can even become negative. When this happens, the good functioning of the neighboring pixels is disturbed. The Vref voltage thus allows us to set a limit for the minimum value of the voltage at node Vd.

The comparator consists of CMOS inverters and NAND gates that are tailored to suit minimal power consumption and comparator noise margin requirements. In read or write mode, the comparator as well as the photo-detector must be disabled. This is achieved by setting the Read/Write Enable (R/WE) input to a high
logic level. In this case the node Vd is connected to gnd and the comparator output remains at the low logic value.

The pulse generator block uses a SRAM memory structure to create a short width pulse. The comparator output signal Vc is connected to the ANDORI structure through two different paths: a direct path and through the SRAM memory as shown in fig.3(b). The difference in the transit time between the two signal paths is detected by the ANDORI which produces a pulse whose width is fixed by the delay time and depends essentially on the dimensions of the access transistor M2 through its $C_{gs}$ Capacitance. Setting $L = 1\mu m$, $W = 1.4\mu m$ and the others transistors to minimum size, the pulse delay is around $0.5\,\text{ns}$, which is sufficient for writing data into the 4-bit SRAM memory.

The 4-bit SRAM memory integrated into the pixel is used to store the current state of the common Gray code counter during the acquisition mode before it is read out during the read mode using two buses: a primary data bus and a complementary one in order to avoid deterioration to the signals. Readout is done row by row under the control of the Row Read/Write (RR/W) signal.

5. SENSOR OPERATION

In this section, we describe the three main phases in the capture of a single frame. These phases are: a write or initialization phase, an acquisition phase and a read phase.

Write phase

Before an acquisition is done, all the pixel memories must be initialized with a default value. In this way, all the pixels that have not received enough luminous flux in order to latch the current value of the grey code counter during the acquisition phase would have as value the default value. To write the default value in the pixel memories, we have to, first, write it in an internal register of the FSM, then make it available on the complementary bus before it is stored in the pixel memories under the control of the (RR/W) signal. At each step, the correct operation code must be applied to the Cde inputs.

Acquisition phase

Before the acquisition of an image really starts, three rising clock edges are necessary so as to set the correct value for the reset, init and Read/Write Enable signals. These signals are used to initialize the photo-detectors, and to activate the pulse generator. At the fourth rising edge of the clock, the integration phase and the common 4-bit Gray code counter are simultaneously started. Acquisition is over when the counter has made one turn that is after 16 clock edges. The 4-bit grey coded values ($N_P$) stored in the pixel memories during the acquisition represent the time the moving object passes in front of the pixels. These time durations depends on the frequency of the clock and can be calculated according to the following equation:
\[ T_s = \frac{1}{f} \times N_P(s) \] (1)

Read phase

During this phase, data stored in the pixel memories are read out at the outputs of the chip. Column amplifiers are necessary to perform the readout operation because of the high parasitic capacitance value of the column buses. The random initial state of the column buses will deteriorate the memorized value when the memory access transistors pass from OFF to ON state. To prevent this, the read cycle is executed as follows: firstly, when the access transistors are OFF, the parasitic capacitance \( C_{bus} \) is charged to Vdd volts, next the complementary bus is set to the high impedance state (HIZ). Finally, the access transistors are turned ON, resulting in a potential difference between the two columns that is a function of the value stored in the pixel memories. The column amplifiers detect this potential difference and furnished a logic value that is latched and then readout through the \( 256 \times 4 \) demultiplexer.

6. TEST

The DPS chip has been tested and shown to be fully functional. In the following subsections, we briefly describe the test that we have carried out on both stationary and moving objects, and on highly luminous phenomenon and present the results obtained.

Stationary object

The first test that we have realized consists in the acquisition of the image of a stationary object in 16 grey levels fig.4(a). This test has permitted us to verify that the sensor is fully functional. In this case, our sensor operates like a classical image sensor and the grey level of the pixel depends only on the quantity of luminous flux received.

Moving objects

We have considered in the first place the displacement of the spot on an oscilloscope screen. The time base was set to \( 2ms/cm \) which corresponds to a displacement speed of the spot of \( 5m/s \). An image of the spot was taken with a clock frequency of \( 800Hz \) which means that the time difference between two consecutive grey levels is \( 1/800s \). Furthermore, knowing that the sensor was placed at a distance of 50 cm from the oscilloscope screen with a lens of focal length (25mm) and that the size of the pixel is \( 49.2 \mu m \times 49.2 \mu m \), we can deduce the true distance travelled by the spot and thus calculate the speed of the spot. We obtain a speed of 4.94 m/s which is in good agreement with the setting of the time base.

Next, we have considered a laser spotlight fixed on an electrical motor. The angular speed of the electrical motor was previously determined using a tachometer, this speed is \( 1473rpm \). The diameter of the circle formed by the revolving laser spotlight is \( 9.4cm \) that gives a speed of \( 7.24m/s \). The image obtained with a clock frequency of \( 20KHz \) as shown in fig.4(c) has allowed us to calculate the speed of the spotlight, we have found a speed of \( 7.19m/s \). Again the result obtained is quite satisfactory.

Highly luminous stationary phenomenon

During laser soldering, the interaction of the laser beam with the processed material provokes a high release of luminous energy. Local variations of this luminous scene can provide useful information about the associated physical phenomena. A fast video camera that can provide up to 32,000 frames/seconds is used to observe the interaction, however the sampling rate is not high enough to observe all phenomena. In this application, the phenomenon under study is very luminous and the thermal gradient is in fast evolution, for all these reasons our device is well suited for the study of such phenomenon. We have used our sensor to study the power distribution in the spotlight in a static application, the result of different acquisitions is shown in ( fig.4(d), 4(e), 4(f)) the grey level distribution gives directly the information about the power distribution. The advantage of our sensor over the fast video camera is that we can achieve an image of the soldering zone with a very short acquisition time.
Figure 4. a: static 16-gray image b: spotlight speed 10m/s c: speed of laser spotlight 7.19m/s d,e,f: Laser soldering images at three different acquisition rates

7. CONCLUSION

We have described a Digital Pixel Sensor (DPS) based chip implemented in a standard digital CMOS 0.6µm process. The core of the 400 thousand transistor chip is an array of $64 \times 64$ DPS pixels. Each pixel is composed of a photodiode circuit, a comparator, a pulse generator and a 4-bit SRAM. It contains 55 transistors for a pixel size of $49.2 \times 49.2 \mu m$. The acquisition rate of our sensor has been tested up to 1 MHz with pixel reset and A/D conversion performed in parallel for all pixels. The experimental results show that the DPS structure can capture moving luminous object and furnishes an image that contains both temporal and spatial information. From this unique image the speed of the moving object can be calculated with a good accuracy.

REFERENCES